🡪FPGA Synthesisable Verilog code for traffic light:-

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 18.04.2023 14:52:51

// Design Name:

// Module Name: tlc

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

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// Name:-Akul Verma

//Roll No.:-21PHC1R04

//Traffic Light Control

module tlc(

input clock,rst,x,

output reg [1:0] hwy,cntry

);

//states

integer count=25'd100;

wire clk;

parameter S0= 4'b000; //hwy= G , cntry=R

parameter S1= 4'b001; //hwy= G , cntry=R

parameter S2= 4'b010; //hwy= G , cntry=R

parameter S3= 4'b011; //hwy= G , cntry=R

parameter S4= 4'b100; //hwy= G , cntry=R

//output parameters

parameter R=2'b00; //Red

parameter Y=2'b01; //Yellow

parameter G=2'b10; //Green

//Internal states

reg [2:0] c\_state; //current state

reg [2:0] n\_state; //next state

userclock(clock,clk);

initial

begin

n\_state=S0;

c\_state=S0;

hwy=G;

cntry=R;

end

always @(posedge clk)

begin

if(rst==1)

begin

c\_state=S0;

n\_state=S0;

hwy=G;

cntry=R;

end

else

begin

c\_state=n\_state;

case(c\_state)

S0:

if(x==1)

begin

n\_state=S1;

hwy=Y;

cntry=R;

end

else

begin

n\_state=S0;

hwy=G;

cntry=R;

end

S1:

begin

repeat(count)

begin

n\_state=S2;

hwy=R;

cntry=R;

end

end

S2: begin

repeat(count)

begin

n\_state = S3;

hwy=R;

cntry=G;

end

end

S3:

if(x==1)

begin

n\_state=S3;

hwy=R;

cntry=G;

end

else

begin

n\_state=S4;

hwy=R;

cntry=Y;

end

S4:

begin

repeat(count)

begin

n\_state=S0;

hwy=G;

cntry=R;

end

end

default:

begin

repeat(count)

begin

n\_state=S0;

hwy=G;

cntry=R;

end

end

endcase

end

end

endmodule

module userclock(input clock,output clk);

reg clk\_out=0;

reg [25:0] count=0;

always @(posedge clock)

begin

count<=count+1;

if (count==9500000)

begin

count<=0;

clk\_out=~clk\_out;

end

end

assign clk=clk\_out;

endmodule